I Claim:

1. A searcher device for correlating a first code sequence with a second code sequence, the searcher comprising:

a memory for storing the first code sequence; and

a plurality of computation circuits coupled to the memory, wherein each of the plurality of computation circuits performs a correlation operation between the first code sequence and the second code sequence at a unique phase offset.

2. The searcher recited in Claim 1 further comprising:

a plurality of threshold detector circuits, each of the plurality of threshold detector circuits respectively coupled to one of the plurality of computation circuits, the plurality of threshold detector circuits for determining if its respective computation circuit yields a result that exceeds a threshold value.

3. The searcher recited in Claim 1 wherein each of the plurality of computation circuits include components for performing a correlation operation, and an integrate and dump operation.

4. The searcher recited in Claim 1 wherein the plurality of computation circuits is coupled in parallel to the memory.

5. The searcher recited in Claim 1 wherein the searcher is implemented in a code division multiple access (CDMA) communication device.

6. The searcher recited in Claim 1 wherein each of the plurality of computation circuits has a unique coupling offset from each other with respect to a location in which they are coupled to the memory.

7. The searcher recited in Claim 1 wherein the first code sequence is a short PN sequence having an unknown phase and the second code sequence is a locally generated PN sequence with a known phase.

8. The searcher recited in Claim 1 wherein each of the plurality of computation circuits is coupled to a same location in the memory.

9. The searcher recited in Claim 8 further comprising:

a memory buffer coupled to at least one of the plurality of computation circuits, the memory buffer delaying the second code sequence provided to the at least one computation circuit to represent a unique code offset.

10. The searcher recited in Claim 8 wherein the memory buffer has a variable length for generating a variable offset.

11. The searcher recited in Claim 8 wherein the first code sequence is the locally generated PN sequence with a known phase and the second code sequence is a short PN sequence having an unknown phase.

12. In a searcher, a method of determining a phase offset of a signal, the method comprising the steps of:

a) receiving the signal having a first code sequence in a memory;

b) receiving an additional signal having a second code sequence at a plurality of computation circuits;

c) implementing a unique phase offset for the second code sequence in each of the plurality of computation circuits; and

d) correlating the second code sequence having the unique phase offsets with the first code sequence in each of the respective plurality of computation circuits.

13. The method recited in Claim 12 further comprising the steps of:

e) comparing, respectively, the correlation results from each of the plurality of computation circuits with a threshold value at one of a plurality of threshold detectors; and

f) transmitting a signal from any of the plurality of threshold detectors if the threshold value is satisfied.

14. The method recited in Claim 13 wherein steps b) through f) are performed in parallel.

15. The method recited in Claim 12 further comprising the steps of:

e) integrating the results of the correlation steps d); and

f) dumping the results of the integrating step d).

16. The method recited in Claim 12 wherein the first code sequence and the second code sequence are suitable for a CDMA communication protocol.

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17. The method recited in Claim 12 wherein offsetting step c) comprises the following step:

loading the second code sequences in the plurality of computation circuits wherein the plurality of computation circuits are each coupled in an offset manner with the memory.

18. The method recited in Claim 12 wherein offsetting step c) comprises the following step:

temporarily storing the second code sequence in a memory buffer with varying size to provide the unique phase offset to each of the plurality of computation circuits.

19. The method recited in Claim 12 wherein offsetting step c) comprises the following step:

receiving a unique offset version of the second code sequence at each of the plurality of computation circuits.

20. The method recited in Claim 12 further comprising the steps of:

e) locally generating, the first code sequence in the communication device; and

f) receiving the second code sequence from a transmitting device.

21. The method recited in Claim 12 further comprising the steps of:

e) locally generating, the second code sequence in the communication device; and

f) receiving the first code sequence from the transmitting device.

22. The method recited in Claim 12 further comprising the step of:

e) locally scaling, an input system clock rate to a local clock rate via a local controller, the local clock rate communicated to components in the searcher.

23. A communication device for processing data signals, the communication device comprising:

a transceiver for receiving a signal having a first code sequence;

a code source for generating a second code sequence; and

a searcher coupled to the transceiver and to a code generator, the searcher having a plurality of computation circuits for correlating in parallel the first code sequence and the second code sequence at a plurality of offsets.

24. The communication device recited in Claim 23 further comprising:

a memory coupled to the searcher, the memory for storing data and program instructions; and

a processor coupled to the memory, the processor for executing the program instructions.

25. The communication device recited in Claim 24 wherein the searcher has a variable phase offset, the memory and the processor providing phase offset data for the searcher.

26. The communication device recited in Claim 23 further comprising:

at least one memory block coupled to at least one of the plurality of computation circuits, the memory block having a variable length to implement a variable offset between the first code sequence and the second code sequence.

27. The communication device system recited in Claim 23 wherein the searcher system is implemented using a code division multiple access (CDMA) protocol.